UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/809,731	03/15/2001	Aaron Giles	068167.0107	5671

7590 10/21/2004

Steven J. Rocci
WOODCOCK WASHBURN LLP
One Liberty Place
46th Floor
Philadelphia, PA 19103

EXAMINER	
SHAAWAT, MUSSA	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 10/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/809,731	GILES ET AL.	
	Examiner	Art Unit	
	Mussa A Shaawat	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *15 March 2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to application # 09/809,731, filed on March 15, 2001. Claims 1-20 are presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Eric P. Traut US Patent No. (6,651,132) referred to hereinafter as Traut.

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As to claim 1, Traut teaches a method for emulating on a computer system the operation of a guest computer system, comprising the steps of: providing an emulation program that runs as an application on the operating system of the host computer system, the emulation program emulating for at least one guest application program the operation of a guest operating system (see col.1 lines 64-67); receiving at the emulation program blocks of software instructions from

the guest application program (see col.2 lines 33-36, et-seq.); and determining, for each block of instructions, whether (a) the block of instructions includes user level instructions, in which case the instructions are passed to the processor of the computer system for execution (see col.4 line 17), or (b) the block of instructions include supervisor level instructions, in which case the block of instructions is translated and the translated block of instructions is passed to the processor of the computer system for execution (see col.4 line 15).

As to claim 2, Traut teaches a method for emulating the operating of a guest computer system on a host computer system of claim 1, wherein the step of translating supervisor level instructions comprises the step of dynamically translating a block of instructions that include at least one supervisor level instruction (col.6 lines 52-58, et-seq.).

As to claim 3, Traut teaches a method for emulating the operating of a guest computer system on a host computer system of claim 1, further comprising the step of saving to a cache the translated instruction (see col.3 lines 5-8).

As to claim 4, Traut teaches a method for emulating the operating of a guest computer system on a host computer system of claim 3, further comprising the step of evaluating for each block of supervisor level instructions to be translated, whether a translation for the instruction block resides in cache memory (see col.3 lines 12-15).

As to claim 5, Traut teaches a method for emulating the operating of a guest computer system on a host computer system of claim 4, further comprising the step of retrieving a translated instruction block from cache memory when it is determined, following an evaluation of cache memory, that a translated instruction block associated with an untranslated block of supervisor level instructions resides in cache memory (see col.3 lines 16-19, et-seq.).

As to claim 6, Traut teaches a method for emulating the operating of a guest computer system on a host computer system of claim 5, wherein the step of translating an untranslated block of supervisor level instructions is performed only if translated instruction block associated with the untranslated block of supervisor level instructions does not reside in cache memory (see col.7 lines 25-35).

As to claim 7, Traut teaches a method for emulating the operation of a guest computer system on a host computer system of claim 6, further comprising the step of passing a series of user level instructions to the processor of the computer system and monitoring the computer system for an exception to indicate a transition from user level instructions to supervisor level instructions (see col.4 lines 25-28, et-seq.).

As to claim 8, Traut teaches a method for emulating the operating of a guest computer system on a host computer system of claim 1, wherein the guest operating system is designed to run on the processor of the computer system (col.2 lines 15—18 and col.1 lines 53-57).

As to claim 9, Traut teaches a method for emulating the operating of a guest computer system on a host computer system of claim 1, wherein the guest operating system is a more recent version of the host operating system (see col.7 lines 35-40).

As to claim 10, Traut teaches a method for emulating on a host computer system the operation of a guest computer system, wherein the application programs of the host computer system and the application programs of the guest computer system can execute on the processor of the host computer system, comprising the steps of: providing an emulation program that emulates the operation of a guest operating system (see col.1 lines 64-67); receiving at the emulation program software instructions from a guest application program (see col.2 lines 33-

36, et-seq.); parsing the instructions into blocks of instructions (see col.2 lines 42-45); determining for each block of instructions whether the block includes supervisor level instructions (see col.4 line 17), wherein each block of instructions that does not include a supervisor level instruction is passed to the processor of the host computer system, and wherein each block of instructions that includes a supervisor level instruction undergoes a translation step before being passed to the processor for execution (see col.4 line 15).

As to claim 11, Traut teaches a method for emulating on a host computer system the operation of a guest computer system of claim 10, wherein the step of passing each block of instructions that do not include a supervisor level instruction to the processor of the host computer system comprises the step of passing user level instructions to the host processor (col.6 lines 52-58, et-seq.).

As to claim 12, Traut teaches a method for emulating on a host computer system the operation of a guest computer system of claim 11, wherein the step of passing user level instructions to the host processor comprises the step of passing user level instructions from a guest application program to the host processor without translation of the instructions (see col.7 lines 25-40).

As to claim 13, Traut teaches a method for emulating on a host computer system the operation of a guest computer system of claim 12, further comprising the step of saving to a cache each translated instruction (see col.3 lines 5-8).

As to claim 14, Traut teaches a method for emulating on a host computer system the operation of a guest computer system of claim 13, further comprising the step of evaluating for

each block of instructions that includes a supervisor level instruction to be translated, whether a translation for the block of instructions resides in the cache (see col.3 lines 12-15).

As to claim 15, Traut teaches a method for emulating on a host computer system the operation of a guest computer system of claim 14, further comprising the steps of, if a translation for a selected block of instructions is in the cache, passing the translated block of instructions to the processor of the host computer system for execution; and if a translation for a selected block of instructions is not in the cache, translating the selected block of instructions and passing the translated block of instructions to the processor of the host computer system for execution (see col.7 lines 25-40).

As to claim 16, Traut teaches a method for emulating on a host computer system the operation of a guest computer system of claim 10, wherein the guest operating system is a more recent version of the operating system of the host computer system (see col.7 lines 35-40).

As to claim 17, Traut teaches a method for emulating on a host computer system the operation of a guest computer system, the guest computer system including guest application program designed to executed on the processor of the host computer system, comprising the steps of: providing an emulation program that runs as an application on the operating system of the host computer system, the emulation program emulating for at least one guest application program the operation of a guest operating system (see col.1 lines 64-67); receiving at the emulation program blocks of instructions from a selected guest application program (see col.2 lines 33-36, et-seq.); parsing each block of instruction to determine whether each block of instructions includes supervisor level instructions (see col.2 lines 42-45), and, for those blocks of instructions that do not include supervisor level instructions, passing the block of instructions

to the processor of the host computer system for execution (see col.4 line 17); and for those blocks of instructions that include supervisor level instructions, translating the block of instructions before passing the translated block of instructions to the processor of the host computer system for execution (see col.4 line 15).

As to claim 18, Traut teaches a method for emulating on a host computer system the operation of a guest computer system of claim 17, further comprising the step of determining, for each block of instructions that include supervisor level instructions, whether a translation for the block of supervisor level instructions exists in cache memory, and for each translated block of supervisor level instructions that exists in cache memory, passing the translated block of supervisor level instructions to the processor of the host computer system for execution (see col.7 lines 25-40).

As to claim 19, Traut teaches a method for emulating on a host computer system the operation of a guest computer system of claim 18, further comprising the step of saving to cache memory each translated block of supervisor level instructions (see col.3 lines 5-8).

As to claim 20, Traut teaches a method for emulating on a host computer system the operation of a guest computer system of claim 17, wherein the guest operating system is a more recent version of the host operating system (see col.7 lines 35-40).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Kahle et al. US Patent No. (5,812,823) Method and system for performing an emulation context save and restore that is transparent to the operating system.

- Earl et al. US Patent No. (5,815,686) Method and apparatus for address space translation using a TLB.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mussa A Shaawat whose telephone number is (703) 605-1372. The examiner can normally be reached on Monday-Friday (8:30am to 5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R Homere can be reached on (703) 308-6647. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mussa Shaawat
Examiner
October 15, 2004

JEAN R. HOMERE
PRIMARY EXAMINER